REMARKS

The specification and claims 11, 14-16, 24, and 28-30 have been amended. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made." Claims 1-10, 12-13, 17-23, 26-27, and 31-37 have been cancelled. No claims have been added. Hence, claims 11, 14-16, 24-25, and 28-30 are pending.

The drawings stand objected to. Concurrently filed with this Amendment is a proposed drawing correction which addresses the Examiner's concerns. Accordingly, the Examiner is requested to review and approve the proposed drawing correction.

The specification stands objected to. The specification has been amended to address the Examiner's concerns. Accordingly, the Examiner is requested to withdraw the objection to the specification.

Claims 19-30 stand rejected under 35 U.S.C. § 112, second paragraph because the limitation "readout circuit" lacks proper antecedent basis. Claims 24 and 28-30 have been amended to recite a plurality of readout circuits. It is respectfully submitted that the pending claims are in full compliance with every paragraph of 35 U.S.C. § 112. Accordingly, the rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

Applicants are grateful for the indication of allowable subject matter in claims 11, 14-16, 24-25, and 28-30. Claims 11, 14-16, 24, and 38-30 have been rewritten as independent claims, incorporating all the limitations of their respective base and intervening claims. As such, claims 11, 14-16, 24, and 28-30 are believed to be allowable over the prior art of record. Claim 25 is also believed to be allowable over the prior art of record as it depends from claim 24.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is

respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

IN THE SPECIFICATION

Please amend the paragraph at page 12, lines 9-21 as follows:

The circuit 52 further includes an analog multiplexer (MUX) 64 which allows the differential value corresponding to a selected one of the pixels to be passed through to a charge transimpedance amplifier (CTIA) 66 which can have a variable gain. The amplified differential signal is stored by another sample-and-hold circuit 68 and is provided to a summing node 70. The summing node 70 also receives signal from a calibration network 72 which uses reference voltages VREF2, VREF3. The output of the summing node 70 is provided to a analog-to-digital converter (ADC) 74 which uses a reference voltage (VREF1). One of more latches 76 store the digital bits and can be enabled to transmit the bits to the bus 54.

Please amend the paragraph at page 20, lines 4-12 as follows:

The amplified differential analog signal then is converted to a corresponding digital signal by the ADC 74. In the implementation of FIG. 4, the ADC 74 includes a comparator 92 and a binary-scaled network of capacitors C11-C18. [C11, C12, C18.] Details of an exemplary comparator circuit 92 are illustrated in FIG. 8. The comparator 92 includes positive and negative terminals and an output. A "strobe" signal enables the comparator 92 to provide an output signal based on the signals at its positive and negative terminals.

Please amend paragraph at page 25, line 16 - page 26, line 8 as follows:

Returning now to FIG. 4, the circuit 52 also includes a calibration network 72 to

provide corrections for the analog-to-digital conversion based, for example, on the offset of the comparator 92. The calibration network 72 also includes a network of small capacitors C19-C26 [C19, C24, C25, C26] whose upper plates are electrically connected to the upper plates of capacitors C11, C12, C18 in the ADC binary-scaled network. Each capacitor C19-C26 [C19, C24, C25, and C26] has a respective latch and logic associated wit. For example, the capacitors C19, C24 have respective latches 102 and logic 100 associated with them and can be connected to either zero volts or a reference voltage VREF2. Similarly, the capacitor C25 has a latch 106 controlled by logic 104 associated with it and can be connected to either zero voltage or the reference voltage VREF2. The capacitor C26 has a latch 110 and controlled by logic 108 associated with it and can be connected to either zero volts or the reference voltage VREF3.

IN THE CLAIMS

Please amend claims 11, 14-16, 24, and 28-37 as follows:

11. [The circuit of claim 10 wherein] A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixel in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network;

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

each of the capacitors in the first capacitor network has an associated latch circuit for storing a bit corresponding to a differential signal for a pixel sampled by the first sample-and-hold circuit while a differential signal for a pixel sampled by the second

sample-and-hold circuit is amplified and converted to a corresponding digital signal.

14. [The circuit of claim 13 wherein] A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixel in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit;

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network; and

a calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network,

the amplified differential output signal from the charge sensing circuit is coupled to

a second input of the comparator, and

the calibration network selectively can be enabled to provide a DC shift to the common node to ensure that the signal for canceling the comparator offset appears as a positive voltage.

15. [The circuit of claim 13 wherein] A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixel in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit;

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network; and

a calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

the calibration network selectively can be enabled to provide a DC shift to the common node to ensure that the signal for canceling the comparator offset appears as a positive voltage.

16. [The circuit of claim 13 wherein] A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixel in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit;

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network; and

a calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

one side of each capacitor in the first capacitor network selectively can be connected to a first reference voltage, and wherein one side of each capacitor in the second capacitor network selectively can be connected to a second reference voltage different from the first reference voltage.

24. [The imager of claim 23 wherein,] A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each circuit includes:

a first sample-and-hold circuit fro sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit fro sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an

amplifier differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

[for each readout circuit,] each of the capacitors in the first capacitor network has an associated latch circuit for storing a bit corresponding to a differential signal for a pixel sampled by the first sample-and-hold circuit while a differential signal for a pixel sampled by the second sample-and-hold circuit is amplified and converted to a corresponding digital signal.

28. [The imager of claim 27 wherein for each readout circuit,] A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each readout circuit includes:

a first sample-and-hold circuit fro sampling and storing signals from pixels in the

first column;

a second sample-and-hold circuit fro sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplifier differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

a calibration network for providing a signal to cancel an offset of the comparator, said calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network, and

the calibration network selectively can be enabled to provide a voltage shift to the common node to ensure that the signal fro canceling the comparator offset appears as a positive voltage.

29. [The imager of claim 27 wherein, for each readout circuit,] A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each readout circuit includes:

a first sample-and-hold circuit fro sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit fro sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplifier differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

a calibration network for providing a signal to cancel an offset of the comparator, said calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network, and

one side of each capacitor in the first capacitor network selectively can be connected to a first reference voltage, and wherein one side of each capacitor in the second capacitor network selectively can be connected to a second reference voltage different from the first reference voltage.

30. [The imager of claim 27, wherein for each readout circuit,] A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each readout circuit includes:

a first sample-and-hold circuit fro sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit fro sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplifier differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said

analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

a calibration network for providing a signal to cancel an offset of the comparator, said calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network, and

the calibration network selectively can be enabled to provide a post-gain offset for the differential output signal from the charge sensing circuit.